A PLANAR-TYPE LOW-NOISE GaAs MONOLITHIC MICROWAVE AMPLIFIER

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ABSTRACT

A planar low noise amplifier has been fabricated by selectively implanting oxygen to define the active devices. Noise figure 2.5 dB with associated gain of 7 dB over the frequency range 4.8-5.3 GHz has been obtained.

Introduction

It is well known that semi-insulating GaAs is suitable to use as a substrate of FET and MIC. If FETs with excellent performance and match elements of circuit are integrated on the same GaAs chip to form MMIC, there results a large reduction in volume and weight of microwave equipment and a great improvement of its original performance.

Usually the mesa structure is used in the fabrication of GaAs MESFET (see Fig. 1a). A great number of limitations occur in technology, such as a fine gate metal strip (0.5-1.0 μm) is easily broken, when it climbs across the mesa edge; the gate pads, match elements of circuit and transmission lines are all laid down on the buffer layer ($n=10^{13}$-$10^{14}/cm^3$), so larger parasitic parameters may be introduced. It is not easy to obtain low noise performance.

In this paper a method of making planar FET and MMIC structure by 0^+-implantation is presented to completely overcome this problem (see Fig. 1b). In this method it is unnecessary to have the gate strip

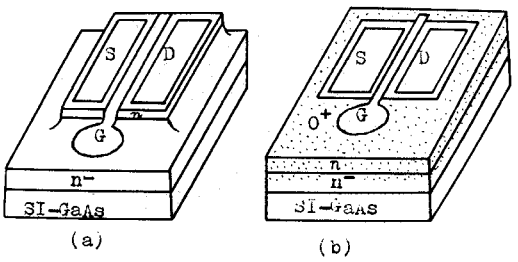

Fig. 1 GaAs MESFET structures (a) mesa type (b) planar type

pass through the mesa step. Planar type technology is much easier to undertake than the mesa type and the most important advantage in the planar structure is its better microwave characteristics.

Consideration of Design

The profile of injected ion in compound semiconductor by ion implantation is quite complicated. In this work we suppose that 0^+ion injecting into GaAs ought to obey Gaussian Profile:

$$N(x) = \frac{\emptyset}{\sigma_p (2\pi)^{\frac{1}{2}}} \exp\left[-\frac{(x-R_p)^2}{2\sigma_p^2}\right] \quad (1)$$

Then, the energy and dose of 0^+ implantation in fabrication planar GaAs FETs and MMIC can be calculated. According to the demand of device fabrication N-layer around the active devices must have semi-insulating characteristics (see Fig. 1b), so the depth of 0^+-implantation must be greater than that of N-layer. It has been shown experimently that the result is good, if the peak of 0^+ concentration at the interface $N\text{-}N^-$ (R_p=a) is used. The implanting energy and junction depth can be obtained from R_p=a.

Suppose an oxygen atom would compensate a carrier, average oxygen concentration must be equal to or greater than the carrier concentration in N-layer. Further the implanted oxygen dose can be obtained. Usually, the gate pad of the FET extends to the buffer layer for mesa type devices. Capacity introduced by gate pad C_p is corresponding to a parallel plate capacitor with gate pad metal as its electrodes and barrier space charge region on GaAs as dielectric. A dependence of capacity per unit gate pad at zero gate voltage on the concentration in buffer layer N_D was calculated. It shows that the gate pad capacity decreases rapidly with the decrease of concentration of buffer layer. For the buffer layer of bad quality (N_D^- = 10^{14}-$10^{15}/cm^3$) the gate pad capacity is too large and the resulting microwave performance of the devices can be heavily compromised. In 0^+-implanted region N_D^- might easily reach 1 x $10^{10}/cm^3$, therefore our 0^+ planar device can bascially eliminate gate pad capacity due to extending of gate pad onto 0^+-implanted GaAs. The isolation of the active region was realized by 0^+ implantation, not mesa etching. The gate pads and match elements of circuit are laid on the 0^+-implanted SI-GaAs layer, not on the buffer layer. For this reason it could be estimated that for MMIC a good isolation between the active devices and match elements, a large reduction of parasitic parameters and microwave loss and further the utilization of the epitaxial layer of perfect crystal lattice with high mobility ($\geqslant$4,500 $cm^2/v\text{-}sec$) for active FET can be provided. By these means a planar low noise monolithic integrated amplifier can be obtained on the basis of 0^+-implanted planar type FETs with good noise figure performance.

Experimental Results

An N^- buffer layer (impurity level $10^{14}/cm^3$) and N-active layer (1 x $10^{17}/cm^3$) was continuously grown on SI-GaAs substrate with an orientation $<100>$ by vapor phase epitaxial method. All the area of GaAs outside the active region of device was multi-implanted by oxygen ion. The range of 0^+ energy is 380-100 keV. The carrier concentration of 0^+ implanted region was lower than $2.5\text{x}10^{10}/cm^3$.

Although the insulating layer with high resistivity was formed, if GaAs after 0^+ implantation had a lot of crystal damage or mismatch, several defects might be formed as a metal impurity aggregating center, which seriously influenced the electric performance and reliability, when it was located around the gate barrier or under the gate pad.

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A backscattering measurement was undertaken. The results showed that crystal lattice rariation damage was very low in the sample annealed at 500° C.

Furthermore using ordinary technology for making planar FET and match circuit, FET with gate length of 1.5 μm and gate wide of 340 μm was designed for our monolithic amplifier. The noise figure of FET is about 2 dB at 6 GHz. The test results of planar and mesa type devices show that the gate capacity of such 0^+-implanted planar type device is 0.2-0.5 pF, smaller than mesa type device using same material. Noise figure is 1-1.5 dB lower and the corresponding gain G_{NF} is 1-2 dB higher.

A planar C-band single stage narrow band GaAs monolithic amplifier was developed by the application of single frequency match technique. The scattering parameters S_{11} and S_{12} of FETs showed that capacitance characteristics appeared at both input and output terminals, so it was necessary to use the inductance elements for the circuit match. Impedance was converted to 50 ohm at input and output. Such matched and converted circuit has been obtained. Due to the selection of frequency range at C-band and the fabrication of the monolithic integrated amplifier on very small size GaAs chip, the lumped elements should be chosen for the match circuit. Ring inductor was used as the match element. Different values of inductance were obtained by the variation of width and diameters of rings.

All three electrodes of FETs are located on the same side of the chip. In order to minimize the distributed parasitic parameter, co-planar transmission line was used, i.e. common ground wire was distributed on the same side of the chip. About 4 μm thick gold layer was electroplated on the surface of the matched elements, connecting wires and the common ground wire to reduce the loss of matched elements, increase the Q-value and maintain the good grounding. Dimension of the chip of single stage amplifier was 1.5 x 1.8 mm^2 (see Fig. 2).

Monolithic amplifier was mounted on the special test jig (see Fig. 3). The DC bias system was designed on the ceramic wafer. The microwave stripline was used to transfer the microwave energy between the coaxial

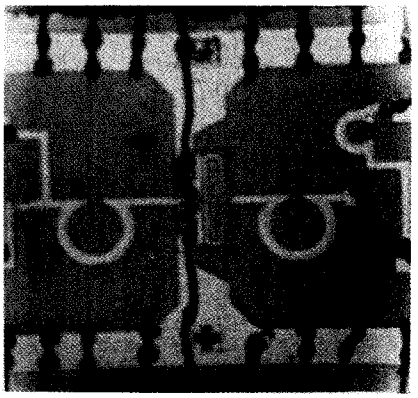

Fig. 2. Chip of monolithic amplifier

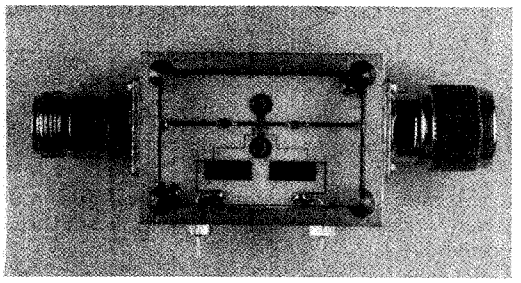

Fig. 3. Monolithic Amplifier and its test jig

connector and the monolithic amplifier. The monolithic circuit microwave stripline and DC bias system were connected by Ø 30 μm wires-bonding. The inductance of bonding wires has been considered in the design, and a revision ought to be undertaken. The connection stripline between the amplifier chip and the common ground wire should be as short as possible. Holes must be made on the ceramic wafer and several bonding wires must be used to ensure the good grounding.

The measurements of microwave performance of the monolithic amplifier showed that 3 dB bandwidth 600 MHz. was obtained, i.e. the frequency range of the amplifier was 4.8-5.3 GHz, while the DC-working point was V_{DS}=3V, I_{DS}= 10 mA. The frequency spectrums of available gain and noise figure are shown in Fig. 4 and 5 respectively. The optimum figure was 2.5 dB and the associate gain $G_a \geqslant 7$ dB.

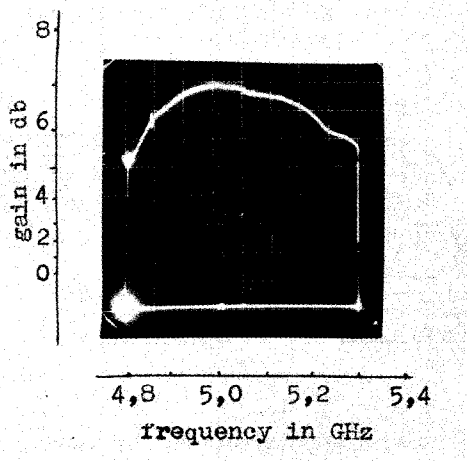

Fig. 4 Gain frequency response of Monolithic amplifier

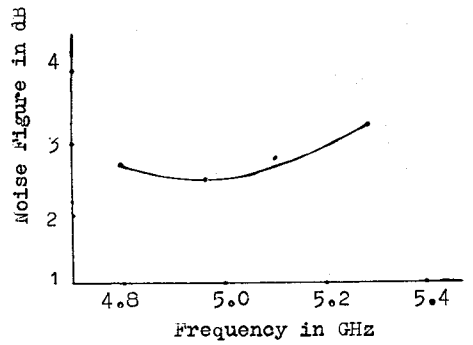

Fig. 5. Noise figure frequency response of monolithic amplifier

Conclusion

Planar C-band low noise FETs and single stage monolithic amplifier have been successfully made by using selective O^+- implantation into GaAs. Such planar MMIC has following significant advantages compared with the ordinary mesa type:

A. The gate pads and match elements of circuit are not set on the buffer layer with carrier concentration of 10^{13}-$10^{14}/cm^3$, but on the O^+-implanted SI-layer with concentration of $10^{10}/cm^3$, so the gate pad capacity was basically illiminated and the microwave circuit loss was greatly decreased. Significant low microwave noise figure and high gain have been obtained.

B. Because of the high flatness of the surface of the wafer the yield of micron and submicron gate metal strip by photolithography was 200% increased. There is no mesa on the GaAs wafer, so no breaking of fine gate metal strip occurs at the mesa edge. Such planar structure is available for making all kinds of GaAs MESFETs and monolithic circuits at any frequency band, such as low noise FETs, Dual gates FETs, Power FETs, monolithic microwave circuit and monolithic high speed logic circuit etc.

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